Design Example Report

Title	***3.3W Non-isolated Flyback converter using DPA423R in 1"x 1"x 0.5"***
Specification	Input: -36VDC to -72VDC Output: 3.3V/1A
Application	Telecom
Author	Power Integrations Applications Department
Document Number	DER-30
Date	March 30, 2004
Revision	1.0

Summary and Features

This report details the design of a flyback converter for bias power supply of hot swap controller unit in switch network system.

- Uses DPA423R
- Non isolated -48VDC input
- No opto coupler
- 1" X 1" board space and 0.5" max component height
- Low Parts Count
- Integrated fault protection including short circuit
- Ceramic output capacitors used for higher reliablity

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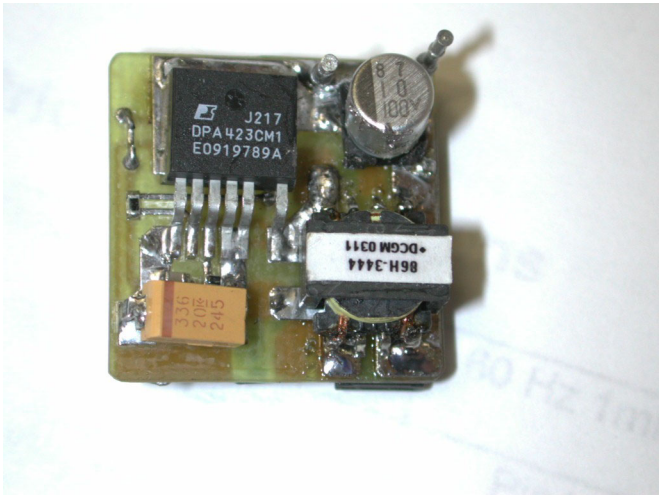
Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolated source to provide power to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

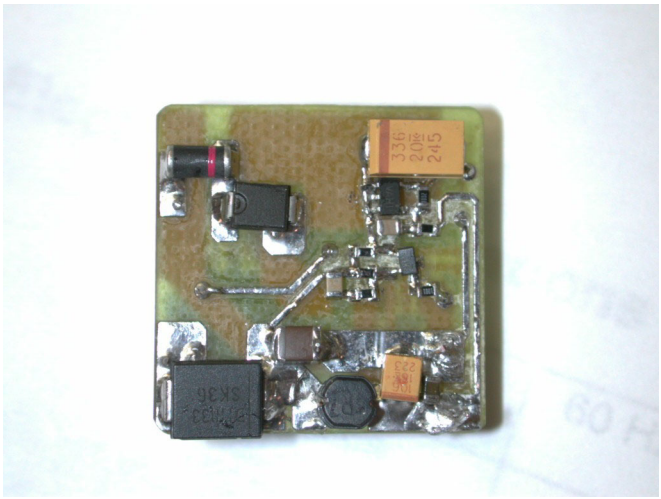
1 Introduction

This document is an engineering report describing a non-isolated single output 3.3W, -48VDC input flyback power supply using DPA423R for bias power supply.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.



Top view



Bottom View

Figure 1 – Populated Circuit Board

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	-36	-48	-72	VDC	
Output						
Output Voltage 1	V_{OUT1}	3.15	3.3	3.45	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}			1	A	90VSC, maximum load
Efficiency	η	65			%	Measured at P_{OUt}, 25 ^{o}C
Ambient Temperature	T_{AMB}			40	^{o}C	Free convection, sea level

3 Schematic

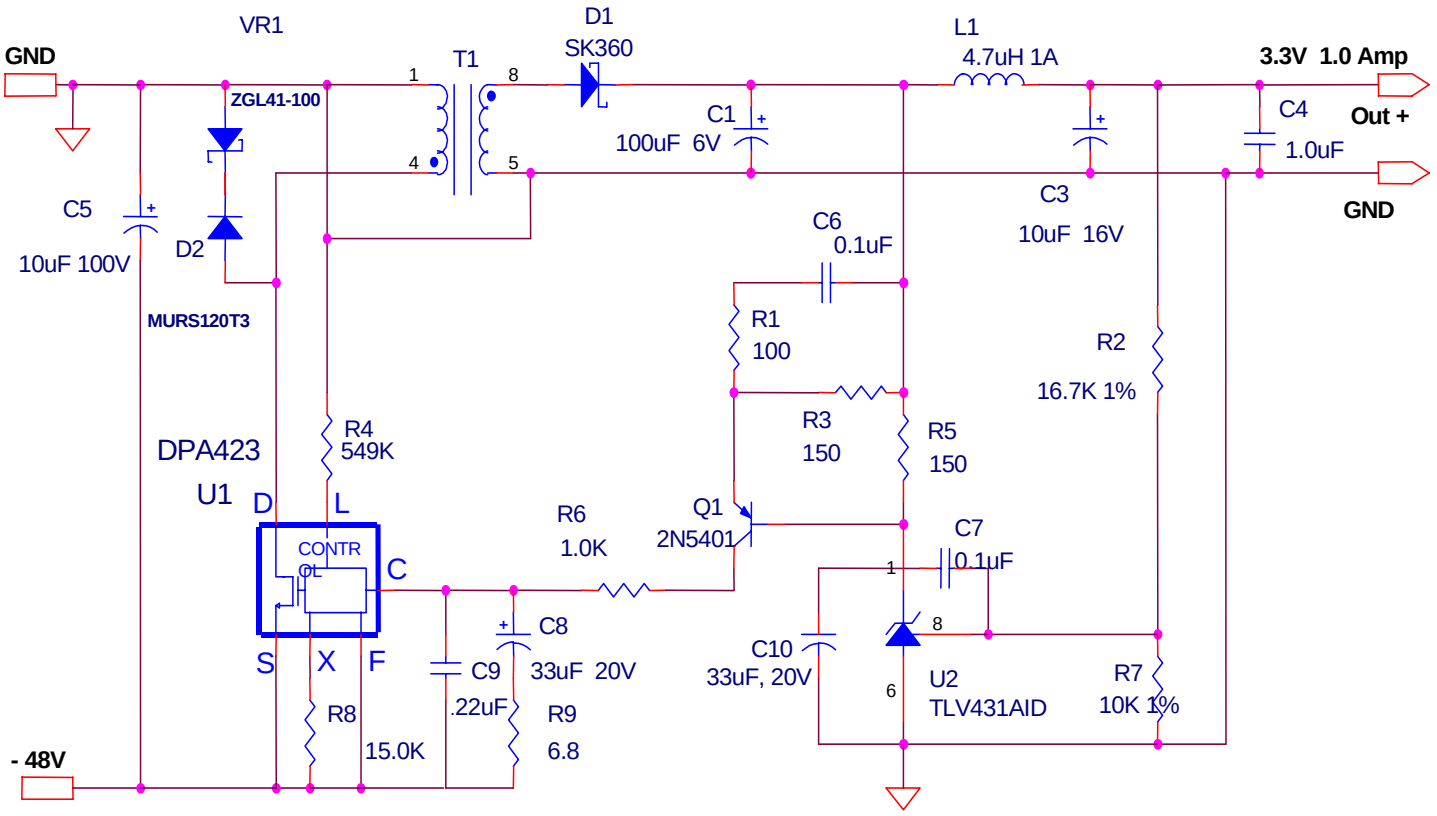

Figure 2 – Schematic

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4 Circuit Description

The schematic in Figure 2 shows a non-isolated 3.3W flyback converter using DPA423R. The circuit is nominally designed for –48VDC input, 3.3V@ 1.0A output

4.1 Primary Side Circuit

The circuit is designed for –36 V to –72 Vdc input range and provides a non-isolated single 3.3V @ 1A output. C5 provides input filtering. The DC rail is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated MOSFET in U1. D2 and VR1 clamp the maximum voltage transients at the Drain of U1 caused by energy stored in the leakage inductance of the transformer.

R4 is used to set the low line turn-on threshold to approximately 33 V, and also sets the over-voltage shutdown level to approximately 88 V. C9 bypasses the U1 control pin, and provides the peak current necessary for driving the ***DPA-Switch*** internal MOSFET. C8 has three functions. It provides the energy required by U1 during startup, sets the auto-restart frequency during fault conditions, and also reduces the gain of U1 as a function of frequency. R9 adds a zero to stabilize the power supply control loop.

4.2 Output Rectification

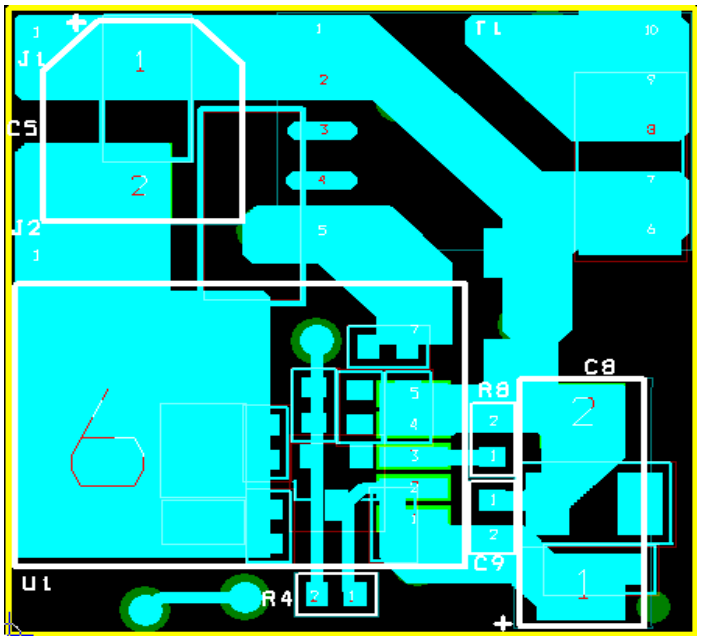
The output of T1 is rectified and filtered by D1 and C1. The inductor L1, C3, and C4 provide additional high frequency filtering for the 3.3V output.

4.3 Output Feedback

Resistors R2 and R7 divide down the supply output voltage and apply it to the reference pin of the 1.25V low voltage programmable shunt regulator U2. The shunt regulator U2 drives PNP transistor Q1 to provide feedback information to the U1 control pin. Components C6, C7, C8, R1, R3,R5, and R9 all assist in compensating the power supply control loop. Capacitor C8 rolls off the gain of U1 at relatively low frequency. Resistor R9 provides a zero to cancel the phase shift of C8. Resistor R3 sets the gain of the direct signal path from the supply output through Q1 and U2. Capacitor C7 rolls off the gain of U2.

5 PCB Layout

TOP Layer



Bottom Layer

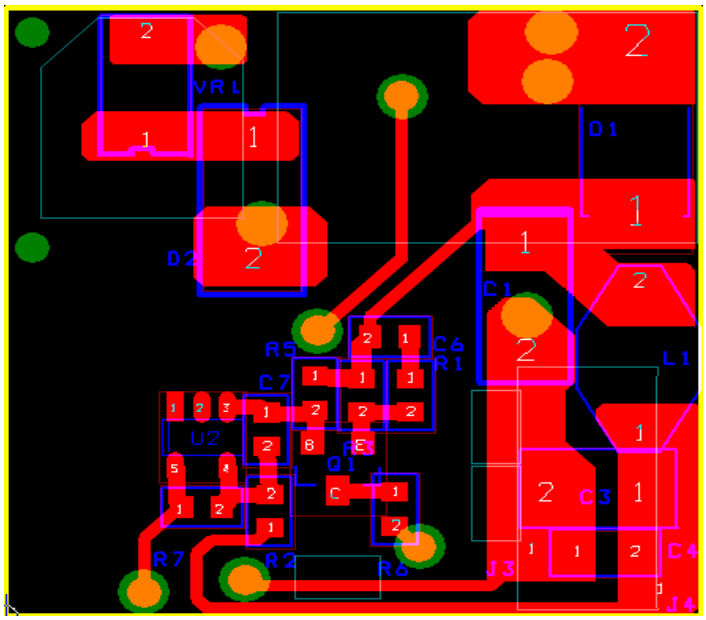


Figure 3 – Printed Circuit Layout

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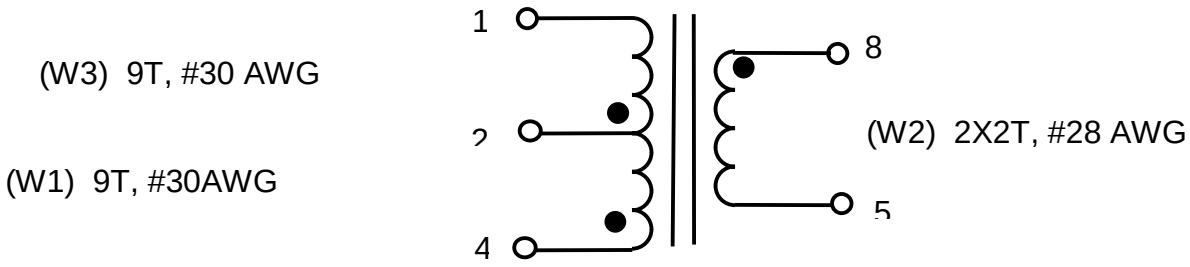
6 Bill Of Materials

Item	Quantity	Reference	Part	Manufaturer
1	1	C1	100uF 10V	Kemet
2	1	C3	10uF 16V	kemet
3	1	C4	1.0uF ceramic	AVX
4	1	C5	10uF 100V	UCC
5	2	C6,C7	0.1uF ceramic	AVX
6	1	C8	33uF 20V	Kemet
7	1	C9	.22uF ceramic	AVX
8	1	C10	33uF, 20V	Kemet
9	1	D1	SK360	Diode inc
10	1	D2	MURS120T3	General semi
11	1	L1	4.7uH 1A	Delta
12	1	Q1	2N5401	On semi
13	1	R1	100	Panasonic
14	1	R2	16.7K 1%	Panasonic
15	2	R3,R5	150	Panasonic
16	1	R4	549K	Panasonic
17	1	R6	1.0K	Panasonic
18	1	R7	10K 1%	Panasonic
19	1	R8	15.0K	Panasonic
20	1	T1	ER11	Delta
21	1	U1	DPA423	Power Integrations
22	1	U2	TLV431AID	National Semi
23	1	VR1	ZGL41-100	Diode inc

7 Transformer Specification

7.1 Electrical Diagram



7.2 Electrical Specifications

Primary Inductance (At 400KHz)	Between Pins 1 - 4 All windings open	74 uH (+/- 5%)
Resonant Frequency	All windings open	1 MHz (Min.)
Primary Leakage Inductance (At 400KHz)	Between pin 5-8 shorted	<3.0uH

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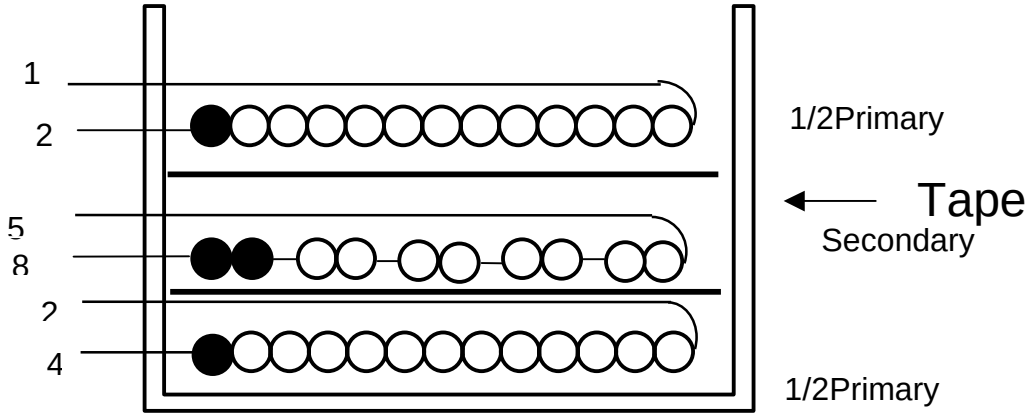
7.3 Transformer construction



7.4 Winding Instructions

1/2 Primary Layer	Start at Pin 4. Wind 9 turns of item [3] from left to right. Finish on Pin 2.
Basic Insulation	1 Layer of tape [5] for basic insulation.
Secondary Winding	Start at Pin 8. Wind 2 bifilar turns of item [4] from left to right. Finish on Pin 5.
Basic Insulation	1 Layer of tape [5] for basic insulation.
1/2 Primary Layer	Start at Pin 2. Wind 9 turns of item [3] from left to right. Finish on Pin 1.
Final Assembly	Assemble and secure core halves. Impregnate uniformly [6].

7.5 Materials

Item	*Description*
[1]	Core: ER11-3F3
[2]	Bobbin: 8 pin ER11 surface
[3]	Magnet Wire: #30 AWG Heavy Nyleze
[4]	Magnet Wire: #28 AWG Heavy Nyleze
[5]	Tape: 3M 1298 Polyester Film
[6]	Varnish

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8 Transformer Spreadsheet

	A	B	D	F	G	I
1	**DAPSwitch_Flyback 090302 rev1e; Copyright Power Integrations Inc. 2002**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**DPASwitch_Flyback_090302 - Continuous/Discontinuous mode Spreadsheet. Copyright 2002 Power Integrations**
2	**ENTER APPLICATION VARIABLES**					**Description**
3	VDCMIN	36.00			Volts	Minimum DC Input Voltage
4	VDCMAX	72.00			Volts	Maximum DC Input Voltage
5	VO	3.30			Volts	Output Voltage
6	PO	3.30			Watts	Output Power
7	n	0.70				Efficiency Estimate
8	Z			0.70		Loss Allocation Factor, (0.7 Recommended)
9	VB	12.00			Volts	Bias Voltage (Recommended between 12V and 18V)
10						
11	**UV AND OV PARAMETERS**					
12			min	max		
13	VUVOFF		29.34	32.36	Volts	Minimum undervoltage On-Off threshold
14	VUVON		31.45	33.86	Volts	Maximum undervoltage Off-On threshold (turn-on)
15	VOVON		73.07	-	Volts	Minimum overvoltage Off-On threshold
16	VOVOFF			92.37	Volts	Maximum overvoltage On-Off threshold (turn-off)
17	RL			603.15	k-Ohms	
18						
19	**ENTER DPASWITCH VARIABLES**					
20	***DPASWITCH***	**dpa423**			*16VDC*	*36VDC*
21	*Chosen Device*	*DPA423*		*Power Out*	*7.5W*	*18W*
22	ILIMITMAX	*1.16*	*1.34*		Amps	From DPASWITCH Data Sheet
23	Frequency	**F**				Enter 'F' for fS = 400KHz and 'L' for fS = 300KHz
24	fS	400000.00			Hertz	DPASWITCH Switching Frequency
25	**VOR**	**35.00**		**35.00**	Volts	Reflected Output Voltage
26	KI	0.70		0.70		Current Limit Reduction Factor
27	ILIMITEXT			0.81	Amps	Minimum External Current limit
28	RX			11.00	k-Ohms	Resistor from X pin to source to set external current limit
29	VDS	2.50			Volts	DPASWITCH on-state Drain to Source Voltage
30	VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
31	VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
32	**KRP/KDP**	**1.10**				Ripple to Peak Current Ratio (0.2 < KRP < 1.0 : 1.0< KDP<6.0)
33						
34	**ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES**					
35	**Core Type**	**ER11**				
36	**Core Manuf**					
37	**Bobbin Manuf**					
38	*Core*		*ER11*		*P/N:*	*ER11-3F3-S*
39	*Bobbin*		*ER11_Bobbin*		*P/N:*	*
40	AE			0.12	cm^2	Core Effective Cross Sectional Area
41	LE			1.47	cm	Core Effective Path Length
42	AL			1200.00	nH/T^2	Ungapped Core Effective Inductance
43	BW			1.85	mm	Bobbin Physical Winding Width
44	M	0.00			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
45	**L**	**2.00**				Number of Primary Layers
46	**NS**	**2.00**				Number of Secondary Turns
47						
48	**CURRENT WAVEFORM SHAPE PARAMETERS**					
49	DMAX			0.49		Maximum Duty Cycle
50	IAVG			0.13	Amps	Average Primary Current
51	IP			0.54	Amps	Peak Primary Current
52	IR			0.54	Amps	Primary Ripple Current
53	IRMS			0.22	Amps	Primary RMS Current

	A	B	D	F	G	I
55	**TRANSFORMER PRIMARY DESIGN PARAMETERS**					
56	LP			74.20	uHenries	Primary Inductance
57	NP			18.42		Primary Winding Number of Turns
58	NB			6.68		Bias Winding Number of Turns
59	ALG			218.67	nH/T^2	Gapped Core Effective Inductance
60	BP			2748.64	Gauss	Peak Flux density exceeds 4000 Gauss. Increase NS, Increase VOR
61	BM		***Warning***	1819.97	Gauss	Peak Flux density<2000 Gauss, A smaller core may be used
62	BAC		***Warning***	909.98	Gauss	Limit AC Flux Density to less than 650 Gauss for limiting Core losses, Reduce BM, Reduce VOR
63	ur			1179.62		Relative Permeability of Ungapped Core
64	**LG**			**0.06**	mm	Gap Length (Lg >> 0.051 mm)
65	BWE			3.70	mm	Effective Bobbin Width
66						
67	**TRANSFORMER SECONDARY DESIGN PARAMETERS**					
68	ISP			4.95	Amps	Peak Secondary Current
69	ISRMS			1.95	Amps	Secondary RMS Current
70	IO			1.00	Amps	Power Supply Output Current
71	IRIPPLE			1.68	Amps	Output Capacitor RMS Ripple Current
72						
73	**VOLTAGE STRESS PARAMETERS**					
74	VDRAIN			165.50	Volts	Maximum Drain Voltage (Includes Effect of Leakage Inductance)
75	PIVS			11.12	Volts	Output Rectifier Maximum Peak Inverse Voltage
76	PIVB			38.13	Volts	Bias Rectifier Maximum Peak Inverse Voltage

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9 Performance Data

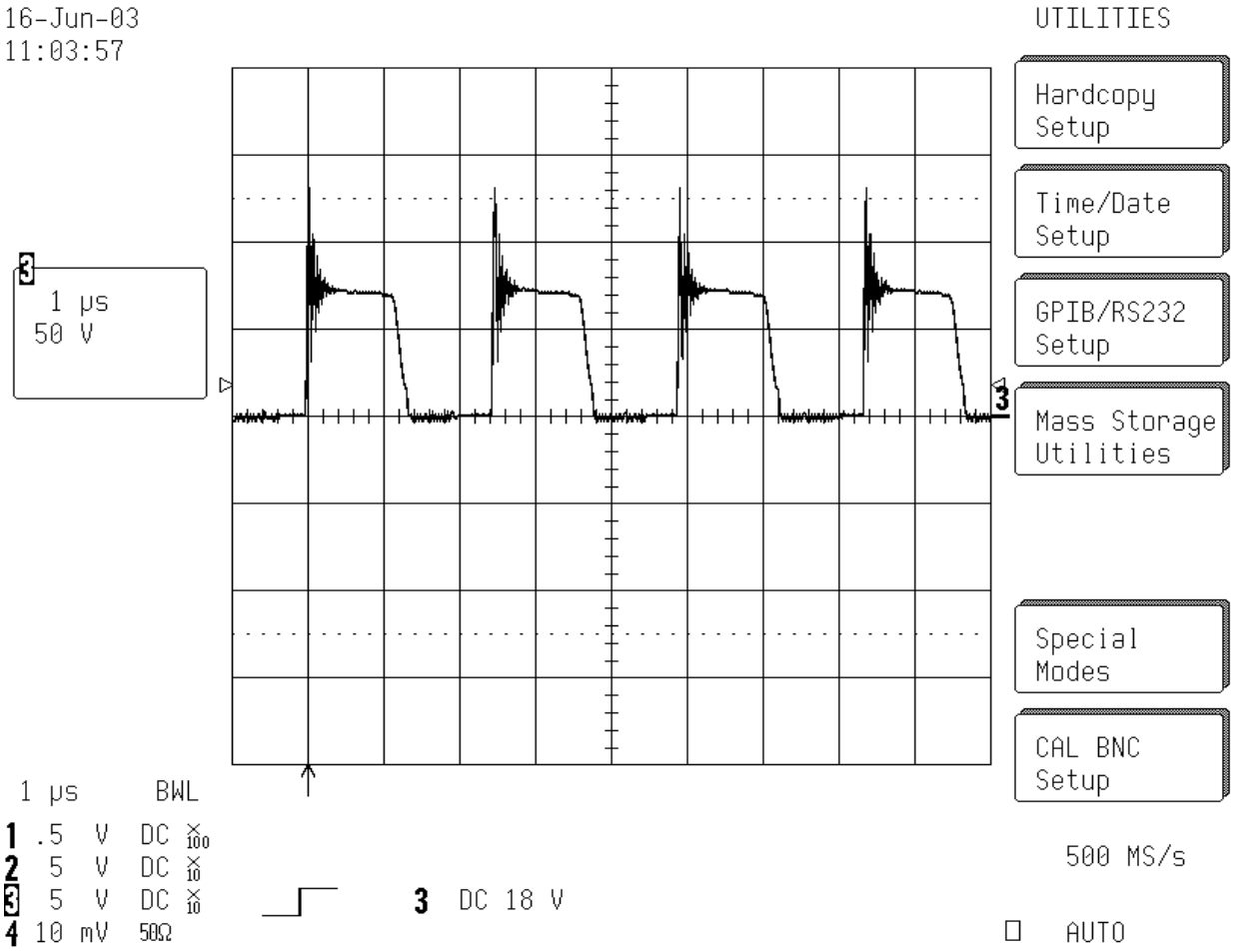
All measurements unless otherwise stated performed at room temperature, 60 Hz input frequency.

9.1 Power Efficiency:

	Input Voltage (V)	Input Current (A)	Output Voltage (V)	Output current (A)	Pin (W)	Pout (W)	Efficiency (%)
No Load	-36	0.009	3.32	0	0.32		
	-48	0.008	3.32	0	0.38		
	-72	0.007	3.32	0	0.50		
Full load	-36	0.12	3.32	1	4.32	3.32	77%
	-48	0.095	3.32	1	4.56	3.32	73%
	-72	0.065	3.32	1	4.68	3.32	71%

10 Waveforms

10.1 Drain Voltage waveforms



Drain to Source voltage waveform at Vin=36VDC, Vout =3.3V @ 1A

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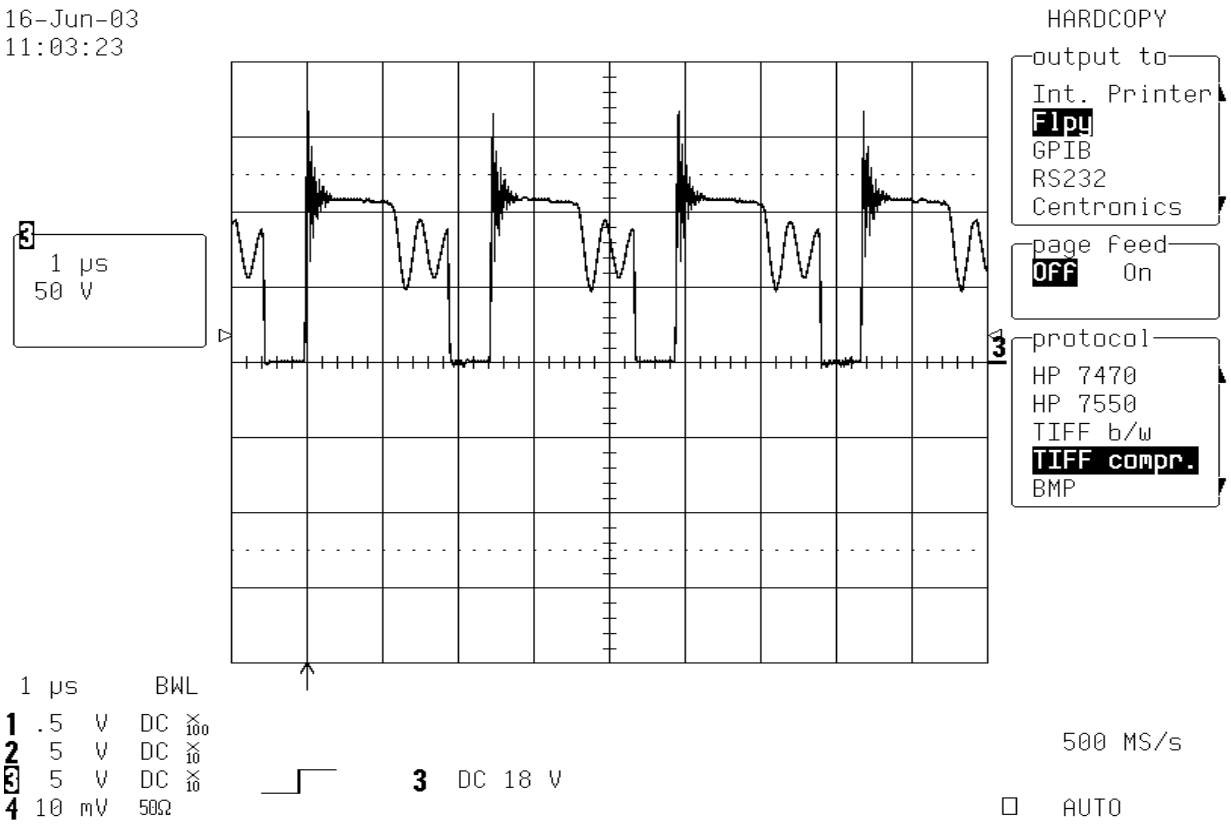
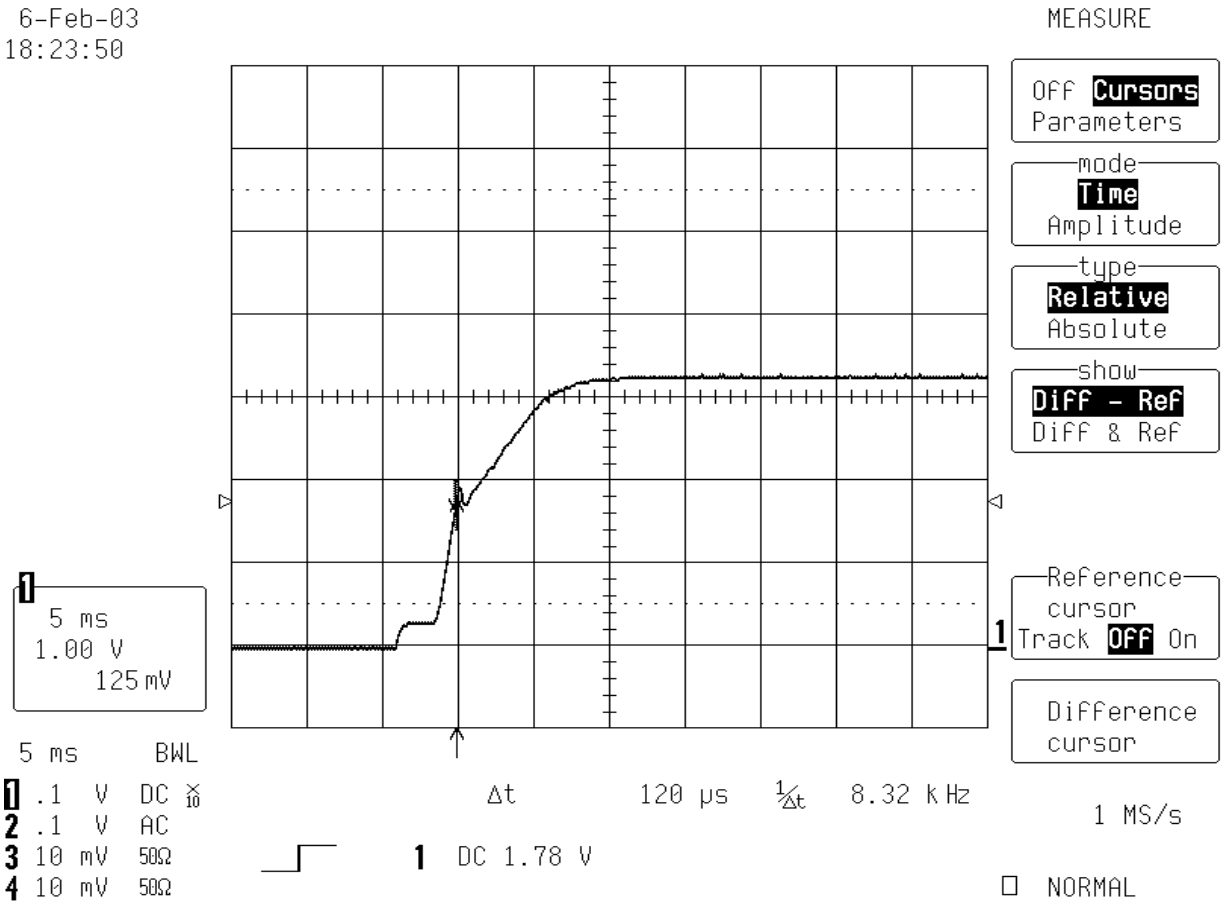


Drain to Source voltage waveform at Vin=72VDC, Vout =3.3V @ 1A

10.2 Start up voltage waveform



3.3V output start up voltage waveform at Vin = 48VDC, Load =3 ohms

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10.3 Output Ripple Measurements

10.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 4.

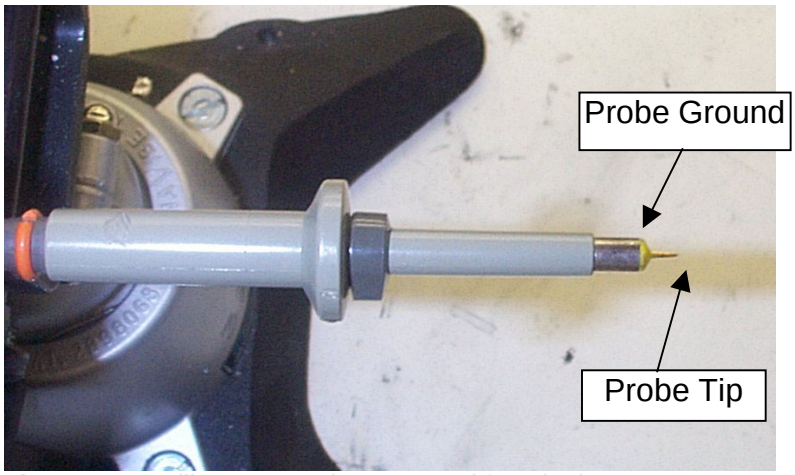
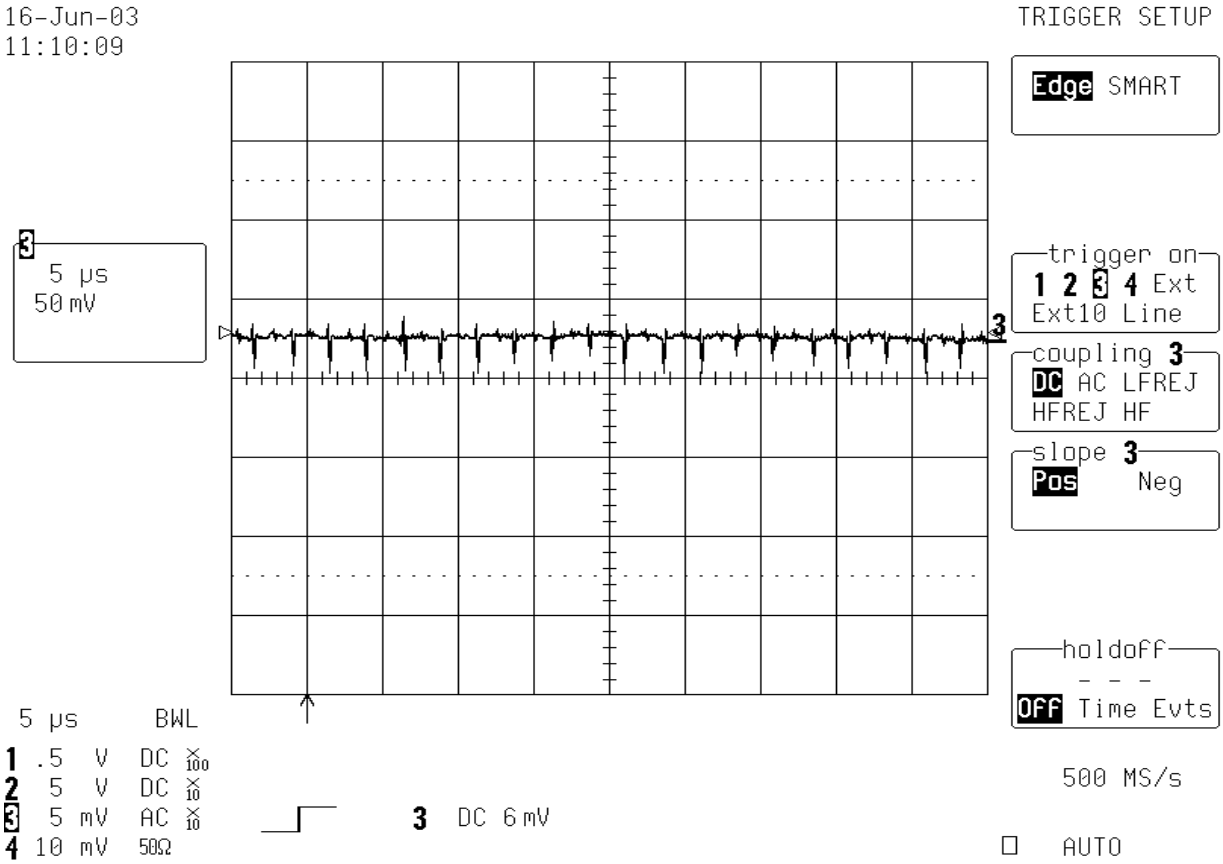


Figure 4 - Oscilloscope Probe Prepared for Ripple Measurement.
(End Cap and Ground Lead Removed)

10.3.2 Measurement Results



3.3V ripple voltage waveform at -36VDC input and 1A loaded output

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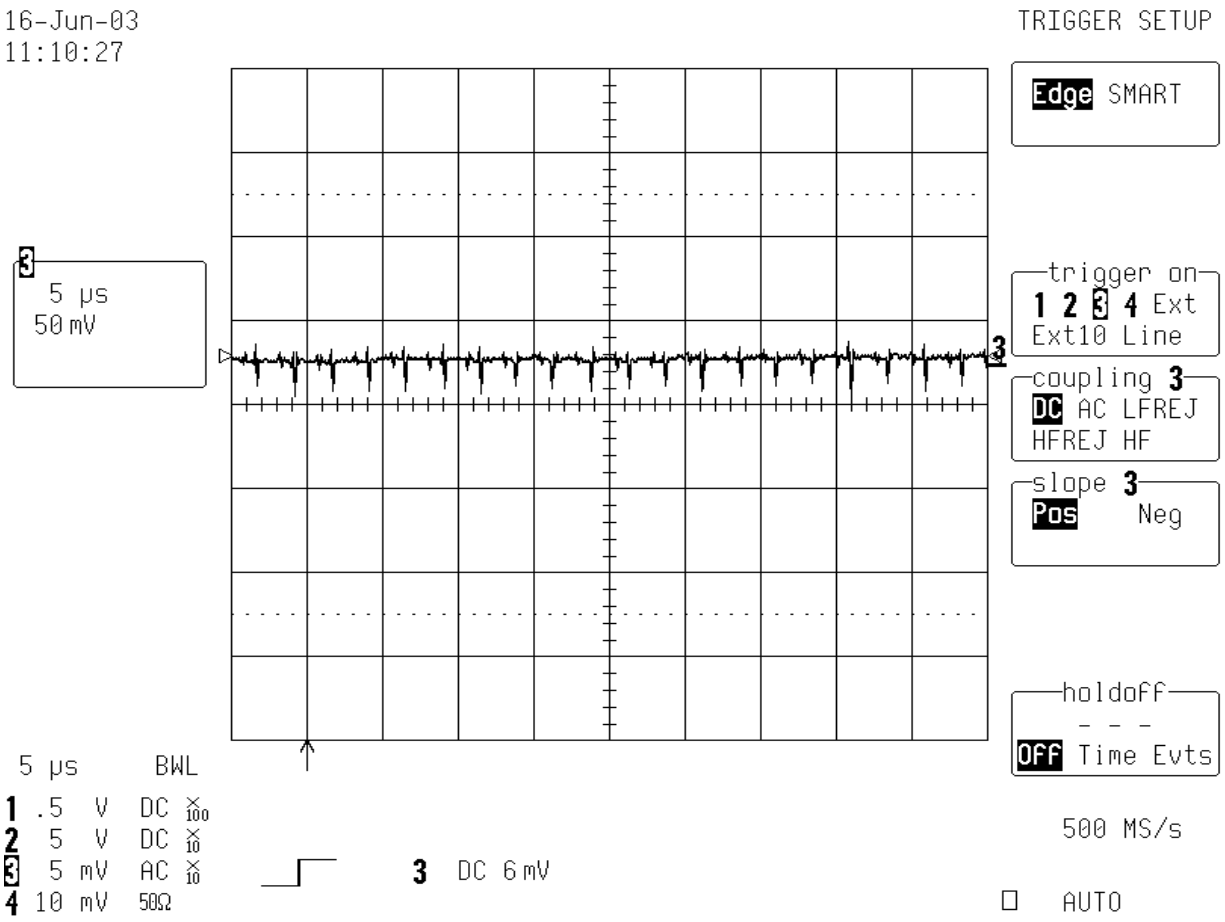
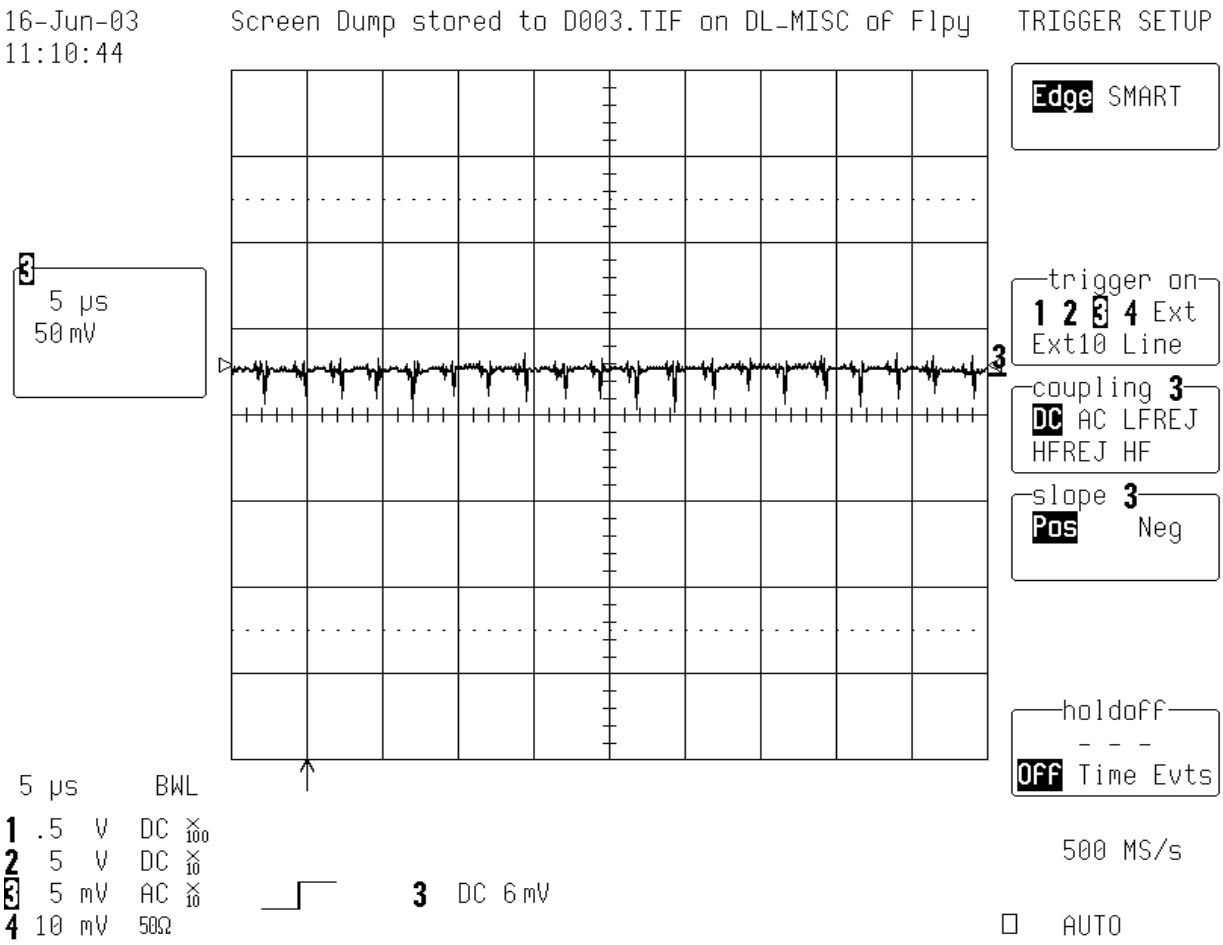


3.3V ripple voltage waveform at -48VDC input and 1A loaded output



3.3V ripple voltage waveform at -72VDC input and 1A loaded output

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11 Revision History

Date	Author	Revision	Description & changes	Reviewed
March 30, 2004	DK	1.0	Initial release	VC / AM

Notes

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